Listing of Claims

The following listing of claims will replace all prior versions, and listings, of claims in the subject application:

Claims 1-2 (canceled).

3. (previously presented) A subcode-data generating circuit, which generates subcode data including subcode component data which indicates time information and additional subcode component data which indicates information other than the time information, said circuit comprising:

a first generating portion for automatically generating the subcode component data which indicates the time information;

a second generating portion for automatically generating the additional subcode component data which indicates the information other than the time information;

a selecting portion which selects an output of at least one of said first and second generating portions; and

a memory,

wherein said first generating portion operates according to a first command for automatic generation of a plurality of time information subcode component data,

wherein said second generating portion operates according to a second command for automatic generation of a plurality of additional subcode component data, and

wherein the first commands are written collectively in a first area of said memory, and the second commands are written collectively in a second area of said memory.

4. (previously presented) The subcode-data generating circuit, as claimed in claim 3, wherein:

said second generating portion comprises a plurality of generating portions provided separately;

said second area of said memory comprises a plurality of areas corresponding to said plurality of generating portions; and

commands of the second commands are written collectively in each area of said plurality of areas, which commands correspond to a respective one of said plurality of generating portions.

5. (currently amended) A subcode-data generating circuit, which generates ~~and selects~~ subcode data including subcode component data, ~~a state of said subcode component data alternating between a high state and a low state at a predetermined period,~~ said circuit comprising:

a toggle generating portion which independently generates ~~subcode component~~ toggling data, the state of said ~~subcode component~~ toggling data alternating between ~~the~~ a high state and ~~the~~ a low state at ~~the~~ a predetermined period; and

a selecting portion which selects one of the subcode component data and the toggling data of said toggle generating portion~~,~~

~~wherein the state of said subcode component data alternates between the high state and the low state at the predetermined period, based on a number of data sectors corresponding to the subcode component data prior to the alternation~~.